MICRONET INNOVATIONS (2000–2001)

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**Device Innovations**

**D1 Thin Film Capacitors Based on Ferroelectric Materials**
S. Delprat, M. Chaker, H. Pépin (INRS-Énergie et Matériaux), M. Ouaddari and K. Wu (École Polytechnique de Montréal)

An *in-situ* process (electrodes and ferroelectric material deposition, annealing) has been developed in the context of the fabrication of Pt/BST/Pt capacitors. This has resulted in the improvement of the dielectric constant from \(\varepsilon_r = 250\) to \(\varepsilon_r = 550\) for 200 nm-thick BST films. In addition, a CAD model of interdigital capacitors (IDC) has been developed for the determination of the microwave dielectric properties of the ferroelectric thin films deposited on dielectric substrates. In this model, a conformal mapping technique is used to evaluate closed form expressions for the computation of capacitances of IDC on layered substrates. The relative dielectric constant \(\varepsilon_r\) of the ferroelectric thin films can then be calculated, from the geometry of the IDC, the thickness of the ferroelectric film, the thickness and dielectric constant of the substrate and the measured capacitance.

**D2 A New Plasma Model for Sputter-Etching of Platinum**
S. Delprat, M. Chaker and F. Vidal (INRS-Énergie et Matériaux), L. Stafford and J. Margot (Université de Montréal)

Measurements of the sputter-etching characteristics in our low-pressure high-density plasma reactor show that, as the gas pressure increases, the etch rate drastically decreases (especially above 1 mTorr), while the ion density of the bulk plasma increases up to about 5 mTorr. To understand this unexpected result, we have introduced the concept of sputtering efficiency defined as the etch rate divided by the ion density. A simple model shows that this sputtering efficiency increases linearly with the ion density at the sheath edge rather than with that of the bulk plasma. It is the change in the shape of the ion density profile in the vicinity of the surface that results in an ion density at the sheath edge always decreasing with increasing pressure, irrespective of the bulk density. As a consequence, optimization of the etch rate requires operation in the very low pressure regime, 1 mTorr or so.

**D3 Reactive Pulsed Laser Deposition of High-k Silicon Dioxide and Silicon Oxynitride Thin Films for Gate-Dielectric Applications**
E. Desbiens, R. Dolbec and M.A. El Khakani (INRS-Énergie et Matériaux)

We have successfully developed two reactive pulsed laser deposition (PLD) processes for the growth of high-k SiO\(_2\) and SiO\(_x\)N\(_y\) thin films. At a KrF laser intensity of 3\(\times\)10\(^8\) W/cm\(^2\), both SiO\(_2\) and SiO\(_x\)N\(_y\) films have been deposited by ablating a silicon target in a reactive gas atmosphere (O\(_2\) and O\(_2\)/N\(_2\) mixture, respectively) on both Si (100) and Pt-coated Si substrates. We have particularly pointed out the effect of both (i) the deposition temperature (in the 20-450°C range) and (ii) the N incorporation (in the 0.3-20 at.% concentration range) on the microstructure and electrical properties of PLD SiO\(_2\) and SiO\(_x\)N\(_y\) thin films, respectively. For the PLD-SiO\(_2\) films, 300°C has been identified as the optimal deposition temperature that yields stoichiometric ([O]/[Si] \(\approx\) 1.9), hydrogen-free films with a low local disorder, a highly dense microstructure and a dielectric constant (k) higher than that quoted for thermally grown SiO\(_2\). On the other hand, the PLD SiO\(_x\)N\(_y\) films containing 20 at.% of N have exhibited a dielectric constant as high as \(~7\). A good agreement was obtained between the k values deduced from the Poole-Frenkel emission.
(PFE) model and those obtained from direct impedance measurements, confirming thereby that the PFE remains the predominant conduction mechanism in the PLD SiO_xN_y films.

**D4 Ultra-Sensitive Capacitance Sensor**  
D.J. Thomson, G.E. Bridges, D.R. Oliver and T. Tran (University of Manitoba)

Capacitance is often measured for diagnostic and sensor applications. As part of this subproject we have developed a capacitance sensor that is a considerable advancement over present sensors and is capable of “zeptofarad” (10^-21 F) capacitance measurement resolution. This sensitivity is based on experimental data and simulation results that are in excellent agreement. The sensor is particularly useful in the Scanning Capacitance Microscopy where our sensor enables cross-sectional imaging of semiconductor devices at a resolution that has not previously been possible. This technology has been licensed to a Micronet industrial partner (Iders) and is now being sold under the trade name "ZeptoScan”.

**D5 Copper Inductors Boost Integrated Circuit Performance**  
J.R. Rogers, V. Levnets, C. Pawlowicz, N.G. Tarr, T.J. Smy and C. Plett (Carleton University)

Copper metalization is now appearing in leading edge integrated circuit technologies offered by some major companies. However, many otherwise advanced process technologies still offer only aluminum metalization. We have developed a simple technique based on electroless plating to add copper inductors to commercial integrated circuits fabricated in processes providing only aluminum metalization. The copper is plated over a thick layer of polyimide added to improve electromagnetic isolation from the substrate. Copper inductors formed in this way provide peak Q values close to 20, while Q values of 6 are normal for aluminum inductors. The ability to form high-Q inductors has been exploited to significantly reduce the noise of voltage controlled oscillator (VCO) circuits designed in Nortel’s high speed NT25 bipolar technology. Using copper inductors, phase noise was improved by 4 dBC/Hz compared to control circuits with aluminum inductors. This allowed the noise specifications for GSM communication systems to be met for the first time in an integrated circuit. This work was reported at the IEEE Custom Integrated Circuit Conference and in *IEEE Transactions on Electron Devices*.

**D6 Deep Submicron, Low Voltage CMOS Imagers**  
J. Fortier, A. Swaminathan, N.G. Tarr and C. Plett, (Carleton University)

Imagers using CMOS pixel arrays are finding increasingly widespread use, CMOS imagers can be fabricated in generic digital processes at low cost, and digital signal processing capability can be integrated on the same chip as the pixel array. However, the reduction in power supply voltage required as CMOS technologies scale towards the 0.1 μm generation poses severe challenges for imager design, particularly in terms of dynamic range. A new strategy for CMOS imager design, radically different from existing approaches, is presented here to meet these challenges. Second order sigma-delta modulator based analog-to-digital conversion is used to read each pixel. By using sigma-delta modulation for A-to-D conversion, pixel saturation under bright light conditions can be detected, and the time elapsed between refresh and saturation recorded. This strategy greatly increases optical dynamic range. This technique was implemented in a 4 by 4 test array fabricated in 0.18 μm technology. The imager provided a remarkable five orders of linear intrascene dynamic
range while operating from a power supply of just 1.2 V. A-to-D power consumption was just 60 µW. This work was reported at the 2001 European Solid State Circuits Conference.

**D7  RF MOSFET Noise Extraction and Modeling**  
C.H. Chen and M.J. Deen (McMaster University)

In this research, we developed a framework to characterize the noise of deep-submicron MOSFETS. It includes test chip design, parameter de-embedding, noise calculation based on any complicated equivalent circuit model, noise source extraction directly from the RF noise measurements, noise modeling of channel noise, induced gate noise and their correlation for circuit simulators and benchmark circuit design for model verification.

This work extracts the noise currents of deep-submicron MOSFETs directly from RF noise measurements as a function frequency, bias condition and channel length. These results can serve as direct targets for the groups doing the RF noise modeling of MOSFETs and can provide a guide line for RF circuit designers to design low noise, RF circuits in the absence of an accurate noise compact model.

This work provides a general and complete solution for the noise characterization of any kind of active devices - not only for MOSFETs. The techniques used in the test chip design, parameter de-embedding, noise parameter calculation and noise source extraction can also be used in the noise characterization of BJTs, HEMTs, MODFETs, HBTs and other RF active devices.

**D8  RF MOSFET Reliability Studies and Implications**  
S. Nasek, R. Murji and M.J. Deen (McMaster University)

As dimensions of microelectronic devices shrinks to smaller values, CMOS technology becomes increasingly popular for RF applications. By decreasing the device dimension, however, hot carrier problem becomes more important. Therefore it is important to be aware of the hot carrier reliability issues in RF circuits made with submicron CMOS technologies.

By studying the effects which are caused by hot carriers in the single devices and by highlighting the mechanism by which circuit performance (such phase noise of oscillators, gain and noise figure of amplifiers) is affected, it becomes clear what issues need to be looked at the circuit design stage or even designing new device structures.

Results of this work make clear in which directions the next research works should be conducted (e.g., circuit design techniques, device structure design) to improve the hot carrier reliability of RF circuits made of CMOS technology.

**D9  A Scalable Meander-Line Resistor Model**  
R. Murji and M.J. Deen (McMaster University)

We have developed a scalable meander-line resistor model which will allow integrated circuit designers to properly use these resistors for RFICs up to 15 GHz. The significance of this research is that the model is accurate up to 15GHz, and since it is in a meander line configuration, it saves area on the chip as compared to a straight line resistor. Since modeled in the metal layer of silicon, it has lower noise when compared to other types of
resistors in silicon. Other researchers would be interested in such a model because of its scalability and its adaptability to other semiconductor technologies.

D10  A 1V, 1.9 GHz Mixer Using a Lateral Bipolar Transistor in CMOS  
S. Ye, K. Yano and C.A.T. Salama (University of Toronto)

A RF mixer using the lateral bipolar transistor inherent in CMOS was designed and fabricated in a standard 0.25μm CMOS process. At 1.93 GHz, the mixer has a 6.5 dB gain, a 9.7 dB noise figure and -3.5 dBm IIP3. The circuit draws 1.3mW from a 1V supply. The work demonstrated that a MOSFET and the inherent lateral bipolar transistor can be used to design a low power mixer with good high frequency performance characteristics. Such a mixer is a likely candidate for low power portable wireless applications. The design compares very favorably with previously reported mixers at 1.9 GHz while using a simple architecture, requiring few components, eliminating interstage coupling, offering variable gain control (by adjusting the gate bias of the n-MOSFET) and reducing the supply voltage while still maintaining excellent performance.

D11 Multi-Harmonic Tuning Behavior of MOSFET RF Power Devices  
Y. Zhang and C.A.T. Salama (University of Toronto)

A categorization of the multiharmonic tuning behavior of RF power amplifiers into four basic modes was carried out. Conventional power amplifier modes (Class AB, E, F, etc.) can then be characterized using these modes of operation in so far as multiharmonic tuning is concerned. A systematic multiharmonic tuning optimization procedure was introduced to find the optimum harmonic terminations in power amplifier applications for wireless communications. A simulation and experimental study of the multiharmonic tuning behavior of bulk silicon MOSFET RF power devices identified the specific mode (both odd/even harmonics OPEN) which results in the highest efficiency for such devices.

D12 A Uniform Compact Model for Planar RF/MMIC Interconnect Inductors and Transformers  
J. Long (University of Toronto) and M. Jackson (University of British Columbia)

A physics-based compact model for on-chip transmission lines, spiral inductors and transformers was developed. This SPICE-compatible model includes all important sources of substrate loss and a simplified capacitance model that speeds parameter extraction. Model accuracy is benchmarked with both experimental measurements and numerical simulations. Results were presented at the IEEE-BCTM 2001 last September in Minneapolis, MN.

D13 Millimeter-Wave Characteristics of SiGe Heterojunction Bipolar Transistors and Monolithic Interconnects in Silicon Technologies  
J. Long (University of Toronto) and M. Jackson (University of British Columbia)

A measurement approach for extraction of S-parameters up to several hundred GHz, including the deembedding of access interconnect metallization has been developed and demonstrated. Propagation characteristics for coplanar striplines fabricated in a SiGe technology were measured to 300 GHz, and are in good agreement with 3-dimensional electromagnetic simulations. This work is the first accurately-deembedded S-parameter
measurement made with laser-based electro-optic sampling, and was presented at ISSCC 2001 last February.

**D14 Design of Self-Correcting Active Pixel Sensor**  
Y. Audet (École Polytechnique de Montréal) and G.H. Chapman (Simon Fraser University)

This overview presents some of the results extracted from a paper presented in October 2001 at the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems: "Design of a Self-Correcting Active Pixel Sensor". The work described a novel APS pixel architecture where the gate-controlled lateral bipolar phototransistors would be employed.

This paper has demonstrated the robustness of the self-correcting scheme proposed to improve the yield of a large area APS sensor. It has been shown that the redundant pixel circuit proposed with a simple column amplifier produces ratios of defect free pixel over faulty pixel output voltages of nearly 2.0 for stuck at high and stuck at low types of fault. The value of the ratios represents an ideal characteristic for a simple and fast correction algorithm consisting of only a left bit shift of the digitally converted output from the column amplifier. The ratios have been proven to be stable for different values of photocurrent and over the entire range of integration. Also, we have found that variation of the threshold voltage of one readout transistor of the redundant pixel affected the ratios in less than half the values of threshold voltage variation itself. Based on these simulation results a good level of confidence is expected for this self-correcting scheme implemented on a real device.

**D15 Simulation of Thin Film Growth Using 3D-Films**  
T. Smy (Carleton University), M. Brett and S. Dew (University of Alberta)

The paper entitled "3 D Microstructural Simulation of Thin Film Deposition for VLSI Interconnects" by T. Smy, S.K. Dew, et al presented at the 2000 VLSI Multilevel Interconnection Conference in Santa Clara, CA., on June 27 - 29, 2000, was selected for the 2000 VMIC Outstanding Paper Award. This is the largest international conference in VLSI interconnect and is the second time the group has been honored. In 1997 we were awarded the best poster prize.

This paper presented an overview of the 3D thin film modeling work of the group. The use of the simulation tool 3D-films was demonstrated for the deposition of thin metal films over topography and also for modeling GLAD porous films. 3D-Films is a novel 3D simulator – which models the creation and growth of three dimensional microstructure in vapour deposited refractory films over non-planar topography.
D16  **Thermal Modeling of Integrated Optical Device Using Atar**
T. Smy (Carleton University)

The group has recently developed a thermal modeling tool known as Atar. Initially developed to simulate pure thermal and electro-thermal effects in integrated devices, Atar has recently been applied to active integrated optical devices. As an example to investigate the effect of facet heating in ridge lasers, a self-consistent model that accounts for electro-opto-thermal interaction along the laser's cavity is used. The model consists of the simultaneous solutions of the 3D heat equation and the 1D longitudinal carrier and photon rate equations. This work is currently submitted as G. Romo, T. Smy, D. Walkey, and B. Reid, "Modeling Facet Heating in Ridge Lasers" to the Journal of Applied Physics.
Atar is a fully 3D heat flow solver and is based on Quad tree meshing that allows for great expansion of mesh in three dimensions. Using a Finite Difference or TLM (time domain) methodology and building from layout and a technology description Atar is optimized for integrated VLSI models. It is an extendable modeling framework for Electro/thermal, electro/optic/thermal or Mechanical/thermal modeling. The software extracts a network of thermal resistors (temperature dependant) and power sources and couples in the electrical/optical or mechanical models producing a self-consistent solution.

Figure 1: Atar model of a thermal runaway at facet in a ridge laser. (a) 3D model of facet area. (b) Temperature contours.

D17  A Compact Representation of Thermal Resistance Temperature and Power Effects
D.J. Walkey, D. Celo and T.J. Smy (Carleton University)

The dependence of thermal conductivity on temperature causes a simple, constant thermal resistance model to lose accuracy for devices operating at medium to high power in InP or GaAs substrates or at high powers in a silicon substrate. This effect manifests itself in the dependence of thermal resistance on backside temperature and power dissipation. Although each of these effects can be accounted for using existing analytic methods, a constant value in the thermal subcircuit of a device compact model incorporating electrothermal effects still implies an approximation of operating-point dependence, since there is no feedback to the thermal resistance. The equations themselves also carry an unacceptable computational penalty, so direct implementation is inefficient. In order to solve this problem, a new model has been developed based on linearization of the full equations and casting in a form suitable for implementation in a circuit simulation environment. The model prediction has been compared to measured thermal resistance of devices in an InP substrate with excellent agreement to operating temperature in excess of 400K.

D18  Modeling Heat Flow in Bipolar Transistor Emitter Metal
D.J. Walkey, D. Celo and T.J. Smy (Carleton University)

A new method for modeling heat flow through emitter metal connection in multiemitter bipolar transistors has been developed. The method is based on segmentation of each emitter into smaller units to simplify the substrate thermal representation, which is the limiting factor in full numerical simulation due to the large number of elements required for an accurate solution of heat spreading. The emitter metal is then included using a coarse
finite difference approximation of the interconnect structure. The typical lumped approach, which can only represent a single temperature for each finger, cannot account for the reduction in all maximum temperatures due to the action of emitter metal in allowing spreading to the cooler finger ends. By providing a more physical representation of the emitter temperature profiles, the segmented approach allows a correct behavior of maximum finger temperature changes due to emitter metal to be predicted. The results of the segmented method correlate physically with numerical thermal simulation and predict temperature changes to within 5%.
C1  A Simplified Decision-Directed Threshold Scheme for EPR4 Channel Detection
B.J. Maundy and I.A. Omole (University of Calgary)

Optimum data recovery from digital magnetic recording channels using either the PR4 or EPR4 technique is usually achieved using the Viterbi Algorithm (VA) as a means of Maximum-Likelihood Sequence Detection (MLSD). It is well-known that Viterbi detectors using the ACS (add-compare-select) approach requires constant scaling of the state metrics involved, while the decision-directed threshold approach alleviates this problem with an added advantage of reduced complexity (especially for a two state trellis).

In this research, we have not only shown that the decision-directed threshold approach could be used for the detection of a complex, eight states, five-level output signal channels with inter-dependent cells such as an EPR4 channel, but we will also reveal that a versatile detection scheme could be achieved by using a computationally efficient threshold definition we have developed. Moreover, we have shown that a reduced number of thresholds with simplified updates could be used for EPR4 detection as opposed to earlier proposals available in the literature. Thus the new proposition could provide significant advantages in the analog implementation of an EPR4 detector over existing proposals. Existing low voltage current mode circuits we have developed will be used in the hardware implementation of our EPR4 detector.

C2  A Current Mirror Compensation Scheme for Transistor Mismatch
C. Wang, M.O. Ahmad, M.N.S. Swamy and C. Taillefer (Concordia University)

Current mirrors are essential building blocks in the design of analog signal processing and conversion circuits. The operation accuracy of a current mirror is highly dependent on the matching of the transistor pair. However, the transistor mismatch resulting from the non-uniformity of physical parameter in silicon is unavoidable and produces electrical parameter variations that are usually very weakly correlated. Moreover, the mismatch effect becomes more significant when the currents flowing through the transistor pair are reduced. If the transistors of a current mirror are driven in the weak inversion mode, the mismatch could cause the current mirror to malfunction.

In this project, a CMOS current mirror circuit is proposed to compensate for transistor parameter mismatch. This current mirror operates in a very weak current range with an accuracy of less than 1% for a transistor mismatch of 20%. The circuit compensates for transistor mismatches in geometry, mobility, thermal voltage, or threshold voltage using a negative feedback. The circuit presented may easily be implemented using a single poly CMOS technology.

C3  A High-Performance, Low-Voltage, Body-Driven CMOS Current Mirror
X. Zhang and E.I. El-Masry (DalTech, Dalhousie University)

Modern sub-micron CMOS technologies with larger second order effect such as channel length modulation, body effect and lower supply voltage put tremendous challenge in designing high performance analog circuits. Current mirrors (CM’s) are the basic (and most important) building blocks in analogue integrated circuits. Some current mirrors become obsolete under this trend. Recently, advanced CM structures have been introduced in the literature to overcome the above problems. However, the minimum required input
voltage of the above CM’s depends on the threshold voltage $V_{th}$. They may not be tolerated in low-voltage (below 1V) applications, because the threshold voltage does not scale down proportionally with the maximum possible power supply. A novel high-performance low-voltage CMOS current mirror has been developed. The circuit is based on the body-driven 0.18 µm N-well CMOS technology and implements gain-enhancement technique. It does not have threshold voltage limitation which makes it suitable for low-voltage applications. More than 98% current transfer accuracy over wide dynamic range can be achieved. It also gives extremely high output impedance that makes it suitable for current output stage and ultra low input voltage requirement down to very close to 0V. Simulation results using 0.18 µm N-well CMOS technology confirm the excellent performance of this novel current mirror.

C4 Design, Implementation and Test of a Front-End Preamplifier Dedicated to an Ultrasound Receiver
M. Sawan (École Polytechnique de Montréal)

We proposed a fully integrated front-end preamplifier dedicated to the receiver block of a portable ultrasound image processor device. A new preamplification technique is employed which is based on a logarithmic amplifier and followed by a programmable-gain amplifier. Design, implementation, simulation, sensitivity analysis, and validation of the proposed preamplifier have been completed. The logarithmic amplifier, which is based on a True Logarithmic Amplifier (TLA) technique, largely amplifies small amplitude signals, and moderately the large amplitude ones. The programmable-gain amplifier, built around a Timing Gain Compensator (TGC), is used to compensate signal attenuation caused by its traveling several human body tissues. Those main building blocks of an ultrasonic receiver are realized using CMOS 0.35 µm technology. Spectre simulations of both the TLA and TGC show unity gain bandwidths of 100 MHz and 127 MHz respectively when driving a load of 1pF. Measurement of the fabricated chip are done in our laboratory by using an external digital control part programmed in FPGA and close parameters values are obtained. The total chip area is 7.2 mm$^2$ including the digital part needed to program the TGC.

![Typical ultrasound image processing device](image-url)
C5  On-Chip Test Cores for Mixed-Signal IC Circuits
G.W. Roberts, M. Hafed and N. Abaskharoun (McGill University)

An area efficient and robust integrated test core for mixed-signal circuits has been developed. The core consists of a completely digital implementation, except for a simple reconstruction filter and a comparator. It is capable of both generating arbitrary band-limited waveforms (for excitation purposes) and coherently digitizing arbitrary periodic analog waveforms (for DSP-based test and measurement). A prototype was fabricated in a triple-metal 3.3V 0.35µm CMOS process, and was demonstrated to perform various curve tracing, oscilloscope, and spectrum analysis tasks with an effective sampling rate of 4 GHz. Designed for 8 bits of quantization, it achieves a SFDR of 65 dB at 500 KHz and 61 dB at the Nyquist frequency (20.001 MHz). Through sub-sampling and the use of a high-bandwidth front-end sampling network, effective narrow-band signals extending into the GHz range have been captured in a low-cost CMOS process. The core occupies an area equivalent to only about 7 thousand standard-cell 2-input NAND gates. This work has been awarded the 2000 International Test Conference Best Paper Award sponsored by the IEEE Computer Society and the 2000 Best Paper Award from MICRONET 10th Anniversary Workshop.

C6  Circuits for Precision On-Chip Timing Measurements
G.W. Roberts, N. Abaskharoun and A. Chan (McGill University)

Several circuits for performing on-chip sub-nanosecond signal measurements have been developed. The first is a specialized jitter measurement structure based on a Time-to-Digital Converter. Timing signals are derived from a vernier delay line constructed from a series of 64 inverter circuits. The second is a timing measurement device that has been developed from an array of ring oscillator circuits consisting of a two inverters per oscillator. Due to the nature of this design, it is synthesizable with standard cells and maintains high-resolution timing measurement capability. The first design was successfully implemented in a 0.35µm CMOS process realizing a timing resolution of 18ps, requiring an active area of approximately 5mm². The second design has been implemented in a 0.18µm CMOS process requiring an active area of 0.12mm². The second design is capable of providing timing resolution of 10ps.

C7  Bipolar Circuits in a Standard CMOS Process
G.W. Roberts, G. Duerden and M.J. Deen (McGill University)

A design technique for implementing bipolar circuits in a standard CMOS technology has been developed. Lateral bipolar transistors, inherent in standard CMOS processes, and strongly-inverted MOSFET transistors have been used in this work to map traditional bipolar circuitry into CMOS technology. Several filter prototypes have been fabricated in 0.35µm, 0.25µm and 0.18µm CMOS technologies to demonstrate the feasibility of the proposed approach. Simulations and experimental measurements of the various filter prototypes demonstrate that bandwidths of over 10 MHz and dynamic ranges on the order of 50 dB can be achieved using these devices.
C8  **A 20-GHz InP-HBT Voltage Controlled Oscillator with Wide Frequency Tuning Range**
H. Djahanshahi, N. Saniei and C.A.T. Salama (University of Toronto), S. Voinigescu and M. Maliepaard (Nortel Networks)

A 20-GHz-band differential InP VCO for fiber-optic communications systems was implemented. The design is based on positive feedback on a single-stage differential amplifier. The main advantage of the proposed VCO is the wide tunable frequency range, which can be used to compensate for process or temperature variations when used within a PLL. Other features include low power, low transistor count, and, hence, area efficiency compared to conventional ring oscillator VCOs. The implemented InP VCO has an adjustable frequency range of 45% around its midband frequency, operates from 13.75 to 21.5 GHz and provides two complementary outputs each delivering a measured power level of -2.8 to -8 dBm. Total power consumption is 130 mW at 18.6 GHz and increases with the output frequency. At 1-MHz offset to the carrier, the measured phase noise is -90.0 dBc/Hz and has a slope of about -20 dBc/Hz per decade.

C9  **A 10bit, 50Msample/s, Low Power Pipelined A/D Converter For Cable Modem Applications**
S. Hamedi-Hagh and C.A.T. Salama (University of Toronto)

A pipelined A/D converter, suitable for cable modem applications was developed. The A/D converter implemented in a 0.25µm CMOS technology provides a resolution of 10 bits at a sampling rate of 50MSample/s while dissipating 65mW from a 2.5V supply voltage. The DNL and INL are -0.5LSB and 0.95LSB respectively and the peak SNDR is 57dB. The total area of the prototype is 3.2mm² and the core area of the A/D converter excluding pads is 1.2mm². The design significantly outperform previously proposed A/D implementations for such applications.

C10  **A Wide-Tuning Range Transformer-Based RF CMOS Oscillator**
M. Bury and K. Martin (University of Toronto)

This work involved producing a Voltage Controlled Oscillator with a wide enough tuning range, such that the correct centre frequency can be ensured. This is achieved without compromising the power consumption of the circuit. The work is novel in that a transformer is preferred to an inductor to help maximize this tuning range. The design was fabricated in a CMOS 0.18 µm technology, and has a frequency tuning range lying between approximately 2.0 and 2.7 GHz, drawing 20mA from a 1.8V supply. A staggered tuning range was employed to minimize the effect of noise on the analog control voltage, so the control process is a dual one, with both analog and digital controls. The oscillator produces quadrature outputs which are essential for many transceiver systems. Two chips have been submitted for fabrication. The second design will be tested in December 2001. An outline of this project was presented at the Micronet Workshop 2001.

C11  **Variable 2-6 Level Multilevel DRAM**
Y. Xiang, A. Chan, D. Elliott and B. Cockburn (University of Alberta)

We have designed and implemented a multilevel DRAM scheme that uses charge sharing for reference generation and fast parallel sensing to write and read more than one bit of information on each 1T-1C DRAM cell capacitor. MLDRAM technology offers increased...
storage density at the cost of reduced noise margins, reduced retention time, and more complex peripheral circuitry. The most recent of our test chips has four different operating modes that will permit conventional 1-bit-per-cell DRAM operation to be compared experimentally with 1.6 (3 signal levels), 2 (4-level), and 2.6-bit-per-cell (6-level) MLDRAM operation. The simulation waveform below shows all six signal levels and all five reference levels being first written into cells; then the six signal levels are sensed correctly. Taken together, two cells can store 36 levels, or more than 5 bits.

C12 Combined Hard and Soft Error Correction for File Memories
C. Wickman, D. Elliott and B. Cockburn (University of Alberta)

ECC has been used in memory systems and chips to correct hard errors (e.g. manufacturing defects) and soft (transient) errors. The literature suggests that error correction coding (ECC) could be used simultaneously for both kinds of errors, but no quantitative predictions of performance have been made. Employing ECC in an MLDRAM file memory could correct hard errors, enhancing yield, and improve the anticipated lower reliability due to the reduced noise margins in MLDRAM. Note that, if a Hamming ECC word contains a hard error, no soft errors can be corrected in that word.

We have investigated how the mean time between failures varies as a function of the hard defect count, for a 1Gb memory with a 512b ECC word. We assume that scrubbing (error correction of memory contents) is performed every 1000 seconds (but more frequent scrubbing produces even better results). A soft error rate of 100 failures in time (FIT, failures per billion hours) per chip is considered acceptable for non-safety-critical applications. Despite having thousands of hard defects remaining after applying redundant rows and columns, the underlying memory array can have a 1000 times higher failure rate than acceptable levels and still meet the 100 FIT criterion with the help of ECC.
C13  Clock Synthesis Using a Direct Digital Period Synthesis Approach
Y. Savaria and D.E. Calbaza (École Polytechnique de Montréal)

There is a strong requirement for highly accurate clock synthesis circuits. Some applications such as video synchronization require frequency ratios that are exact as described by the ratios of large prime integers. These applications also require high speed and low jitter clocks. Existing direct digital synthesis circuits address these requirements but are limited to generate output frequencies that are smaller than one third of the input frequency. Considering practical constraints with current technologies for analog filter implementation required with DDS, they are limited to generate frequencies below 200 MHz. A new clock generator architecture capable of generating output clocks that are a multiple of the input frequency was proposed, implemented, and validated. Using novel phase accumulator design, the digital direct period synthesis (DDPS) circuit can generate exact frequency ratios expressed by ratios of arbitrary large primes. As it does period synthesis, it spreads phase shifts over many periods and never produces large phase jumps. The design is composed of digital cells used as mixed signal components and is easier to design than classic DDS. Due to these features, it can be used to synthesize high speed clocks. A 0.25\(\mu\)m micron CMOS technology could be used to generate clocks of 1 GHz or more even though our actual prototype chip was limited to 500MHz, due to the limited degree of physical optimization. As an added feature, the DDPS is agile and can switch from one frequency to another in one cycle thus supporting frequency hopping.

This research was motivated by a requirement of Miranda. It was found that Gennum had very similar requirements. They both sponsored the research that lead to this innovation over the past three years.

C14  Effective Reuse Method
Y. Savaria and L. Loiseau (École Polytechnique de Montréal)

With the growing complexity of integrated circuits that routinely allow integration of systems on chip, reuse of previously developed intellectual property (IP) modules becomes critical. Failure to master this rapidly evolving art will soon translate into a fatal competitive disadvantage. Working in close collaboration with Miranda, design reuse methodologies were studied and distilled into a methodology that suits the needs of that corporation. Original components of the method called redesign for reuse is the partitioning of rules that have little or no negative incidence on design time and those that raise the cost of a module while increasing its design time. With the proposed method, the foundations of a reusable module are laid out from the outset and the expense (cost and delays) can be incurred when their impact can be tolerated. The result is a fully reusable module that is as good or better as a module designed according to a rigid design for reuse methodology. The method reduces risks incurred with rigid design for reuse methods. It can really produce better IP at lower risk since the developers are not forced to incur the full expense of making a module reusable before they really know a module will be reused, and they understand multiple use context for that module. The method was adopted by Miranda, and is now evolving as a component of their internal design methods. It was also offered to CMC to serve as a basis for its System on Chip Research Network.
C15  Fast Lock-in Low Phase Noise Phase Locked Loop
Y. Savaria and Y. Fouzar (École Polytechnique de Montréal)

Phase locked loops (PLLs) are pervasive commodity components that are used everywhere in telecommunication and high frequency microelectronics systems. A problem with the design of PLLs is the contradictory requirements between the supported lock range and the resulting phase noise. These two characteristics must be traded-off one against the other. A new phase locked loop architecture that decouples these two features was proposed and characterized. It exploits a simple idea that consists of combining two independent control mechanisms, an open-loop feed-forward mechanism that calibrates the region of operation with a low-gain closed-loop mechanism that does accurate frequency and phase corrections over a relatively small operating range. The low gain, combined with state-of-the-art circuit design techniques, lead to low phase noise without negatively impacting the overall lock-range, which is controlled by a separate open loop mechanism that comprise a frequency to voltage converter that auto-calibrates the range over which the PLL operate. That auto-calibration can compensate parametric variations that would make low-gain loops impractical. The auto-calibration feed-forward mechanism also accelerates the lock-in process in a way that would only be possible with much noisier PLLs.

C16  Digital Algorithms For Analog Adaptive Filters
A.C. Carusone and D.A. Johns (University of Toronto)

The use of analog adaptive filters in modern integrated systems is limited by the complexity of the analog adaptation hardware and by dc offset effects which limit the adaptation accuracy. Both problems can be addressed by using an analog filter with a digital adaptation algorithm. Three new algorithms have been developed where digital signal processing is used to obtain gradient information with little additional analog hardware. A prototype integrated analog filter was used as a testbed to verify two of the novel algorithms. Gradient descent optimization of analog filter parameters was successfully performed without access to any of the filter’s internal state signals, which was not previously possible. As a result, designers of analog adaptive filters are now free to perform the filter design without being restricted by the requirement of the adaptive algorithm.

C17  Incremental Signaling For Chip-to-Chip Communications
A.C. Carusone, K. Farzan, S. Abdalla and D.A. Johns (University of Toronto)

Differential signaling is often used for digital chip-to-chip bus interconnects because it provides common-mode noise rejection. Unfortunately, differential signals generally require 2N signal paths to communicate N signals. We have proposed a signaling scheme referred to as incremental signaling that requires as few as N+1 signal paths for N signals yet it maintains common-mode noise rejection among adjacent lines. Incremental signaling can be viewed as a partial response signaling scheme but except that the sequence is transmitted in parallel over a bus rather than sequentially in time. As a result, we have also shown that through the use of a modified Viterbi detector, the noise performance of this approach is the same as that for differentially signaling but with only about half the number of signal paths. For example, a 32 bit bus with differential signaling would require 64 pins while incremental signaling only requires 33 pins.
C18 Electrical Adaptive Equalization for Optical Communication Systems
M.M. El Said and M.I. Elmasry (University of Waterloo)

A major fiber impairment in older fiber-optic networks is Polarization Mode Dispersion (PMD). PMD prevents older fiber cable from accurately transmitting signals at high speeds (10 Gb/s and higher). What is making things worse, is that PMD fluctuates randomly with time, thus PMD can reach a few times its measured average value. Of course one can never ignore chromatic dispersion, which is still a major source of distortion that greatly limits the capacity of the optical fiber.

Techniques to combat these impairments can be applied both in the optical and electrical domain and both have to be adaptive so as to cope with the time varying nature of PMD. However, there is a growing interest in electrical techniques since they can offer the advantages of lower cost and smaller size through integration within the receiver electronics.

It was only until the last two years that demonstration of electrical adaptive equalization for 10 Gb/s began appearing in the literature. However, they suffer from two major drawbacks. The first is their unsatisfactory dynamic performance. The second drawback is that the adaptation control was done under software control in a computer, which is expensive compared to an integrated circuit solution. Up to this date nothing is available commercially.

The goal of this work is to implement an integrated 10 Gb/s adaptive equalizer for long-haul fiber-optic communication systems. In order to achieve this goal, a new architecture suitable for Gb/s operation is devised. Preliminary results are promising. A prototype should be completed within a year and a half from now.

C19 On Substrate Coupling Noisquake in System-On-Chip (SOC), Fast Modeling Techniques and a New Methodology
N. Masoumi, M.I. Elmasry and S. Safavi-Naeini (University of Waterloo)

A major problem with substrate crosstalk extraction methods in the literature is their lengthy computational time. This practically renders them useless for large circuits. This paper presents efficient substrate parasitic extraction techniques employing closed-form models derived using a quasi-static approach. We develop an integral equation model based on the Green's theorem utilizing a novel fast-convergent Green's function.

In addition, we propose another modeling technique based on point approximation of the elements of the impedance matrix of the system. Although the proposed techniques speed the parasitic extraction process up, we show that it is unnecessary to run a full substrate parasitic extraction among all the devices for a system-on-a-chip. As such, by applying the new modeling technique to a multi-contact substrate structure, we develop a methodology that is a large-scale solution for substrate parasitic extraction in VLSI and mixed-signal circuits. Moreover, we demonstrate that the coupling among the contacts in a large system decreases faster than an exponential function of the distance among them. Using the proposed methodology, we introduce a decomposed two-contact problem set, associated with the original complex problem. Then, the total crosstalk of a device in the original problem is simply computed from the associated decomposed problem set.
C20  **Low-Power RF Front-End Components in SiGe**  
J. Rogers and C. Plett (Carleton University)

Several advances in RF components in a 50 GHz SiGe process have been demonstrated. These include a voltage-controlled oscillator (VCO) with automatic level control and an image-reject notch filter. The VCO used amplitude feedback to keep the VCO at an optimum level for best phase-noise performance over temperature, process, and frequency variations. Measured performance was close to state-of-the-art (the first version of the circuit had 30% tuning range, phase noise of -97dBc/Hz at 100 kHz offset from the carrier and oscillator current of 4 mA from a 3.3 V supply). More importantly, over a temperature range from -40°C to 100°C and over most of the tuning range, the phase noise remained within a few dB of the best number; without this feedback, the phase noise could degrade by more than 15 dB. The second circuit, the integrated image-reject filter with a notch at 7GHz, was designed to replace the more usual combination of an integrated low-noise amplifier and off-chip image-reject filter. This increases the level of integration, and reduces total power dissipation. Measurements showed good image rejection of 70dB, reasonable noise figure, good passband gain, and good linearity.

C21  **A Low-Voltage Fully-Monolithic SSB Transmitter IC for 5-6GHz WLAN in SiGe BiCMOS Technology**  
J. Long (University of Toronto)

A low-voltage fully-monolithic SSB transmitter IC for 5-6GHz WLAN in 0.18um SiGe BiCMOS technology. Projected specs from a 2.7V supply and draws 7.7mA in full power-on (i.e., transmit) mode and 1.2mA in power-down mode. All RF filtering and I/Q signal generation is on-chip. Output power delivered to a 50 Ohm load is +1.4dBm. This IC uses a novel overlay balun fabricated on-chip to improve efficiency. SPICE models for the balun have also been developed. A poster based on this work won a Best Paper Award at the 2001 Micronet Workshop.

C22  **A CMOS VCO Architecture Suitable for Sub-1 Volt High-Frequency (up to 10 GHz) RF Applications**  
A.H. Mostafa and M.N. El-Gamal (McGill University)

A novel LC-based CMOS oscillator architecture which considerably reduces the supply voltage requirement, while being suitable for high-frequency RF applications, was proposed. This was achieved by altering the structure of the conventional “complementary differential LC circuit” (Fig. 1). In addition to maintaining the features of the original topology, such as a high quality resonating tank, low phase noise, suitability for high frequency operation, and low sensitivity to parasitics, the proposed architecture provides an alternative to overcoming the limited tuning range of back-gate tuning employed in the original structure. This is achieved by varying the bias current of transistors M3-M4 in Fig.2, while compensating for any amplitude variations through the bias of M5.

Two VCO prototypes were implemented in a standard 0.18 μm CMOS process (Fig. 2). They operate using 0.85 and 1-Volt power supplies, which is approximately one third the supply voltage needed by the original topology. The two prototypes consume the lowest power (6-9 mW) compared to other CMOS oscillators operating in the 8-10 GHz range.
frequency range, while maintaining an overall high figure of merit and reasonable tuning range (400-450 MHz).

C23  An All-NPN Class-AB Log-Domain Integrator with Supporting Input and Output Circuitry for Low-Voltage and High-Frequency Continuous-Time Filtering
M.N. El-Gamal and R.A. Baki (McGill University)

A new companding-based (log-domain) integrator circuit capable of operation from a very low-voltage supply (1.2 V) was proposed (Fig. 1). The circuit operates in class AB mode, resulting in an extended dynamic range, and is differential, making it interference resistance. It employs only NPN transistors in the signal path, which makes it suitable for high frequency applications, while being realizable in low-cost bipolar processes - as opposed to bipolar processes featuring high-quality PNP devices.

First, as a proof of concept, two high-quality third-order lowpass filter prototypes were built using this new integrator. One of the two filters reached a maximum operating frequency of 100 MHz, making it the fastest log-domain integrator filter, operating with such very low voltage supply, to be reported to date.
Second, in order to gain industrial acceptance, the performance of filters targeting specific applications, realized using the proposed integrators, was to be evaluated and compared to filters realized using conventional filtering schemes. This was achieved by building and characterizing a seventh-order 0.05\textdegree equiripple linear-phase filter for hard-disk drive applications. Experimental results showed that the stringent system specifications could be met, while consuming considerable lower power (5-13 mW at 70 MHz cutoff frequency), compared to state-of-the-art conventional implementations (120 mW at 100 MHz cutoff frequency).

![Fig. 1](image)

C24 High-Speed Signaling: Limitations and Circuit Issues  
M. van Ierssel and A. Sheikholeslami (University of Toronto)

Our research on high-speed chip-to-chip communication addresses two issues: the signaling limits over PCB traces and the circuit solutions to timing uncertainty in high-speed clock distribution.

We determine the limits of signaling based on communications theory and on transmission line effects of PCB traces. The question we intend to answer is that given a circuit technology and given a fixed input signal power, what is the maximum bit-rate that can be reliably transmitted and received in a system. This information is critical to making optimal architecture choices as bit rates increase. We are currently in the process of preparing our preliminary research results for publication.

Our research on timing uncertainty has focused on the phase-linearity of phase interpolators and jitter in clock buffers. We are currently addressing both issues by evaluating sources of phase non-linearity and jitter.

We believe that addressing both the interconnect and the circuit issues will contribute towards the advancement of the state-of-the-art high-speed communications.
C25  **Micropower CMOS Filters for Hearing Aids Using Dynamic Gate Biasing**  
K. Phang (University of Toronto)

Low-voltage circuit design is being driven by the trend towards lower system voltages in CMOS technology, and by the widespread need for lower power dissipation, especially in portable applications. In this past year, we have developed a low-voltage analog circuit technique based on charge-pumps called Dynamic Gate Biasing (DGB). The technique has been utilized in the design of a low-voltage (1.5V), continuous-time, biquadratic CMOS filter for hearing aids. We investigated how this technique could be used to extend the linearity and useful tuning range of the filter. Current simulation results show that a wide range of filter frequency responses are possible, and the power dissipation of the whole filter has been limited to 10uW. As analog designers look for new ways to meet the challenge of reduced supply voltages, dynamic gate biasing has the potential to establish itself as a general technique for realizing low-voltage analog circuits.

C26  **Test Access Mechanism in System Chips Using a Packet Switching Communication Methodology**  
M. Nahvi, A. Ivanov and R. Saleh (University of British Columbia)

One important challenge in testing core-based systems in systems-on-chip is accessing the embedded cores from the chip boundary. This is referred to as Test Access Mechanism (TAM).

We have identified problems in bus-based TAM architectures apparent in terms of test access time and interconnect length. In addition, to overcome these problems and provide a more effective solution for TAM, a Novel Indirect and Modular Architecture (NIMA) for TAM is proposed in this work, where emphasis is placed on modularity, scalability, generality, and configurability of the architecture to exploit the advantages offered by the re-use paradigm. The key idea in our work is to establish an indirect digital communication path through packet switching connections, analogous to the technology used for the Internet. To that end, we have proposed a TAM architecture based on a packet switching communication network and designed its Network Layer. Moreover, work is concluding on NIMA’s Application Layer.

C27  **Differential Thermal Testing of Integrated Circuits**  
A. Syal and A. Ivanov (University of British Columbia)

As CMOS technologies scale down, background leakage current increases inexorably, primarily due to device sub-threshold leakage. As a result, conventional single-threshold pass/fail IDDQ testing may no longer be valid even for 0.25-micron technology. A number of alternatives to single threshold IDDQ testing have been proposed. A testing technique to complement IDDQ testing that has shown promise is thermal signature testing.

We examined the validity of using temperature as a test observable. Once this was done we investigated differential thermal sensing as a possible way of detecting bridging faults in CMOS gates. Differential sensing provides high sensitivity to temperature changes generated by internal changes of the power distribution due to defects and immunity to ambient temperature changes. Different topologies for such sensors have been proposed targeting bipolar and BiCMOS technologies. We designed CMOS thermal sensors,
simulated and later fabricated such sensors. The novelty of our work lies primarily in the fact that these were the first such sensors to have been developed in CMOS technology. They have the advantage that the performance of the CUT is unaffected by the sensors, as there is no direct electrical loading of the circuit due to them. The concept of these sensors allows non-intrusive, on-line and off-line test and diagnosis capabilities.

C28 **Accurate, Passive and Closed-Loop High-Speed Interconnect Model for General Purpose Circuit Simulators**
A. Dounavis, M. Nakhla and R. Achar (Carleton University)

With the continuously increasing operating speeds, sharper rise times and denser layouts, high-speed interconnect effects such as ringing, delay, distortion, crosstalk, attenuation and reflections are becoming the major bottleneck at almost every level of design hierarchy. These effects, if not predicted accurately at early design stages, can severely degrade the system performance and can profoundly affect the design cycle as well as time to market. At higher frequencies, the lumped interconnect models become inadequate and distributed models based on Telegrapher’s equations become necessary. In order to address the above problem, accurate and CPU efficient time-domain macromodels are developed for distributed transmission line networks. The proposed technique uses closed-form Padé approximation of exponential matrices to compute an analytical stamp for general interconnects, based on the knowledge of its RLGC parameters matrices only. In addition, the proposed algorithm guarantees the passivity of the macromodel, which is a mandatory requirement for oscillation free transient simulations, in the presence of rest of the circuit elements. The proposed method can easily handle interconnects with frequency-dependent parameters and hence can account for skin, proximity and edge effects. Also it can very effectively address the problem of on-chip RC distributed interconnects. The macromodel, while preserving the passivity, provides significant speed-ups compared to the conventional approaches such as method of characteristics or lumped RLC models. Compared to the W-element model widely used in the commercial simulators, the developed model is more accurate, more efficient and most importantly, it guarantees passivity of the model and eliminates spurious oscillations.

C29 **Saving Clock Power**
J. Knight and M. Ali Khan (Carleton University)

Heating from excess power usage is probably the leading obstacle for developing chips for tomorrow. Without innovation large chips will melt their packaging. One of the leading sources of power loss is the clock. A circuit dissipates a small amount of power on each clock cycle, but with clocks running at 2 GHz this small amount becomes large when multiplied by two hundred million. Standard logic circuits do useful computation only when the clock voltage is rising. The falling voltage that must inevitably follow is used only to allow another rising edge. Circuits that do useful computations on both rising and falling edges will save half the clock power, but their designs can be difficult. This research has studied improved design methods using both clock edges. Its highlight so far, is the development of a new clocked storage element that can further reduce the clock power to about 30% of the power used by standard rising-edge clock circuits.
C30 High-Frequency Modeling by Adaptive Sampling
V.K. Devabhaktuni and Q.-J. Zhang (Carleton University)

Neural networks recently gained attention in RF/microwave CAD. Neural networks can be trained using measured/simulated data of microwave devices/circuits. Resulting neural models can be used in place of detailed physics/EM models to speed-up microwave design. Neural model development involves critical issues such as network size and number of training samples. Previously, data generation and neural network training were carried out separately, as no quantitative link between the number of samples and neural model accuracy was available.

We developed a novel automatic sampling algorithm. For a given neural model accuracy, the algorithm automatically determines the number of samples and their distribution in model input-space. The algorithm integrates data generation and neural network training into a single process. It periodically drives the data generator (e.g., simulation software) to increment training and test data sets, whenever additional data is needed. Furthermore, in problems that exhibit both smooth and non-linear behavior in different regions of the model input-space, the algorithm automatically detects the nonlinear regions and generates more samples in such regions. Fewer samples are generated in smooth regions thus making the technique cost-effective. The technique can result in faster neural model development cycles, which in turn, will help to accelerate microwave design.

C31 EM-Based Statistical Analysis and Yield Optimization Using Space Mapping Based Neuromodels
J.W. Bandler, J.E. Rayas-Sánchez (McMaster University) and Q.J. Zhang (Carleton University)

Accurate yield optimization and statistical analysis of microwave components are crucial in manufacturability-driven designs in a time-to-market development environment. Yield optimization requires intensive simulations to cover the entire statistic of possible outcomes of a given manufacturing process. Performing direct yield optimization using accurate full wave electromagnetic (EM) simulations does not appear feasible. Here, an efficient procedure to realize EM-based yield optimization and statistical analysis of microwave structures using space mapping-based neuromodels is proposed.

We have mathematically formulated the yield optimization problem using SM-based neuromodels. A general equation to express the relationship between the fine and coarse model sensitivities through a nonlinear, frequency-sensitive neuromapping has been found.

We illustrate our technique by the yield analysis and optimization of an HTS filter. Here we assume symmetric variations in the physical parameters due to tolerances. Efficient procedures have also been developed for the asymmetric case.
C32 Non-Contact Internal RFIC Probe
C. Falkingham and G.E. Bridges (University of Manitoba)

A non-contact probing instrument capable of performing high-frequency magnitude and phase measurements of the signals inside an RF integrated circuit has been developed. The probe uses micromachined scanning force microscopy probes, operating in a non-contact mode and employing their non-linear Coulomb force interaction with the circuit, to measure internal IC signals with a sub-µm spatial resolution. The probe has demonstrated a 16 GHz bandwidth with a <50 mV amplitude and <8 degree phase resolution over a 25 dB dynamic range. The probe adds a loading of less than a few fF to the circuit and can measure circuits without depassivation of the test points. The probe has been used to measure GaAs MMICs used in telecom systems, providing information such as signal levels at internal stages and ground bounce levels on power rails.

C33 Adjoint Sensitivity Analysis and Optimization with Full Wave EM Solvers
N. Georgieva (McMaster University)

Currently, the design of practical high-frequency structures using full wave electromagnetic (EM) simulators is prohibitively slow and often frustrating. A single analysis takes hours even days of CPU time. In the same time, even the most efficient optimization algorithm would often require hundreds of design iterations. This situation is additionally aggravated by the fact that current full wave EM simulators are not capable of providing design sensitivity information, which is crucial to the gradient based optimization process. To estimate the gradient of the objective function, additional simulations are made whose number equals the number of design parameters $N$. Thus at each loop of the optimization process, $N+1$ full wave EM simulations are needed, which for practical problems leads to enormous computational load. We apply the theory of the adjoint variables to the design sensitivity analysis of structures analyzed by the Method of Moments (MoM) in order to develop a highly efficient HF CAD environment for the
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design of wire and printed antennas. The adjoint sensitivity approach allows the derivation of
the response and its exact derivatives with respect to the design parameters with one
simulation. Thus the time required for the overall design process is reduced approximately
by a factor of \( N + 1 \). The same approach can be applied to any EM solver, which reduces the
problem to a system of linear or non-linear system of equations.

C34  **Design for Test Methods for Digital Circuits at High Levels of Design Abstraction**
N. Nicolici (McMaster University)

Traditional design for test methods (DFT) increase useless power dissipation during test
and are not suitable for testing low power very large scale integrated (VLSI) circuits, since
they lead to lower reliability and cause manufacturing yield loss. To reduce power
dissipation during test, the existing power-constrained test scheduling algorithms, based on
fixed test resource allocation, improve power dissipation at the expense of lower test
application time. On the one hand, it was shown that power conscious test synthesis and
test scheduling algorithms eliminate useless power dissipation. On the other hand, it was
demonstrated that, by exploiting regularity in built-in self-testable (BIST) register-transfer
level (RTL) data paths, an improvement in test application time, BIST area overhead,
performance, volume of test data and test efficiency can be achieved. Therefore, by
combining power conscious test synthesis and test scheduling algorithms with high-level
regularity extraction in BIST data paths into low power test compatibility classes will lead
to simultaneous reduction in test application time and power dissipation. In addition,
considering DFT related issues at RTL and higher levels of abstraction provides the means
for tackling the complexity of timing related defects, by decomposing the design and test
tasks into subtasks of manageable complexity.

C35  **Gate-Level Modeling for SOI Circuits**
F.N. Najm (University of Toronto)

Silicon on Insulator (SOI) technology, especially partially-depleted floating body SOI,
offers higher speeds and lower power dissipation compared to bulk CMOS. One reason for
this is the reduced parasitic capacitance in SOI devices and interconnects. Another is that
the coupling between the gate and body nodes, in response to a rising/falling input to a
logic gate, leads to an abrupt body-voltage increase/decrease that helps change the
transistors threshold voltages in a way that increases the speed of the logic gate. However,
the variability of logic gate delay, arising from the variability of the floating body node,
creates problems for timing verification in that the gate speed varies according to the signal
history, a feature that has been called the **memory effect**. During static timing analysis
(STA), one is forced to make worst-case assumptions about the delay of every logic gate.
Under this project, we have studied the delay variation of SOI gates and how it depends on
the gate context (its input slope and output load), with an aim of deriving instance-specific
delay bounds for each gate. We have developed gate delay macro-models that can track the
changes in gate delay as a function of the signal history. These models enable the
construction of fast gate-level simulators for SOI circuits, which is a key requirement for
reducing the overall design time of SOI integrated circuits.
C36  **Power Grid Analysis and Optimization**  
F.N. Najm (University of Toronto)

The push towards smaller feature sizes in integrated circuit (IC) technology has enabled the integration of increasing numbers of transistors per chip, at much higher levels of performance (circuit or clock speed). With more and more transistors per chip working at higher and higher speeds, the power dissipation of ICs has skyrocketed in the last 10 years. In order to reduce or control the increased power dissipation, supply voltages have come down over the years, from 5V to 3.3V, to 1.2V, and will probably go lower in future. This has led to a situation today where the total current requirements of an IC are close to 100 Amperes. The resulting low-voltage high-current power/ground grid design problem is formidable. Any power supply droop due to IR-drop results in circuit slow-down, so that the power grid is now a performance limiting factor in IC design. Simulation of large (30 million branch) power grids is very expensive both in terms of CPU time and memory. We have developed a multi-grid-like technique for power grid simulation, which achieves over 600X speed-up over standard circuit simulation, with sub-1% error. This new technique combines the best features of both traditional variants of multi-grid techniques, namely the standard multi-grid (SMG) and the algebraic multi-grid (AMG), and has developed in collaboration with IBM Corporation.
Research has been carried out that can enhance the effectiveness of hearing instruments through the use of microelectromechanical (MEMS) devices. The design of a microarray of acoustical microphones in a 3x3 planar array is developed. The array consists of nine capacitive-type microphones and has the overall dimensions of 4x4 mm. The array has been designed for hearing instrument applications and is small enough to fit in the average size ear canal. The microphone array provides a beam forming and steering capability that enables a variable directional sensitivity property. This variable directional sensitivity can be used to minimize the effects of background noise and reverberation that are typically present in an acoustical environment and can also provide the basis for a speaker tracking capability. The theory of beamforming and steering has been applied to a microarray that can be fabricated using the latest MEMS fabrication techniques. A MEMS microactuator has also been designed that allows the acoustical energy to be converted into an electromagnetic field that can exert a force on an implanted magnet on the round window of the cochlea so as to provide a bionic interface without the problem of acoustical feedback. The array is shown in the accompanying figure.

The existing techniques for the design of Bode-type variable-amplitude digital equalizers are limited to the realization of first- and second-order shaping transfer functions only. This research presents a novel synthesis approach for the design of higher-order Bode-type variable-amplitude wave-digital equalizers. The salient features of the resulting wave-digital equalizers are, (a) they permit the continuous variation of the equalizer transfer function from the shaping transfer function to its inverse while requiring one single variable digital multiplier only, (b) they are guaranteed to be bounded-input bounded-output stable for all values of the variable digital multiplier, and (c) they exhibit the important practical feature that a geometrically symmetric change in the value of the variable digital multiplier causes a corresponding arithmetically symmetric change in the logarithmic magnitude-frequency response of the equalizer.
A Novel Technique for the Estimation of Stability in Feedforward and Multiple-Feedback Oversampled Sigma-Delta A/D Converters  
N.A. Fraser and B. Nowrouzian (University of Alberta)

The hitherto techniques for the statistical investigation of the stability in feedforward and multiple-feedback sigma-delta analog-to-digital (A/D) converters are based on the restrictive assumption that the quantizer input signal has a Gaussian distribution. However, in such A/D converters, the quantizer input signal is almost always a weighted sum of Gaussian-like distributed signals, leading to a non-Gaussian distribution for the quantizer input signal. This research is concerned with the development of a novel statistical approach for the stability investigation without making any recourse to the aforementioned restrictive assumption, achieved by employing the Gram-Charlier series to more accurately model the quantizer input signal distribution. This includes, (a) the characterization of the quantizer output signal by taking into account the fact that in the case of stable A/D converters, the constituent quantizer almost always operates in its overload-free region, (b) the determination of the quantizer input signal in terms of the analog input signal and in terms of the estimated quantizer output signal bit pattern, and (c) the determination of the required quantizer input signal moments.

A Self-Synchronization Technique for CCD Time-Delay and Integration Cameras  
C. Baykal, G.A. Jullien, R. Muscedere, M. Ahmadi and W.C. Miller (University of Calgary)

Time Delay Integration is a technology used in line-scan cameras to improve moving image quality in low light and/or rapid image velocity environments. Multiple stages of exposure are progressively combined in a charge-shifting CCD array, to yield a much higher image S/N ratio than is available with a single row of sensors. To synchronize the CCD charge movement to the image velocity, the standard practice is to use the output of a shaft encoder as a measure of the image velocity. We have recently developed an entirely new technique for TDI synchronization using only the direct output signal from the CCD sensor and processing this signal with the limited resources available in a prototype networked camera. We have developed several low complexity algorithms for charge-shift “velocity lock” that can be implemented in a small video-stream FPGA device. Our basic approach for all of the current algorithms is to monitor the energy of the high frequency components of the CCD sensor output and use a form of control system to maintain this energy output at its maximum value. The figure below shows the results of one of our algorithms on the synchronization of a test image. On the left is the unsynchronized image. The two other images show the transition (centre) and synchronized image (right).
S5  **Efficient Fault Tolerant Computing Using Redundant Replicated Moduli**  
L. Imbert, G.A. Jullien and V.S. Dimitrov (University of Calgary)

We have discovered a new technique for the efficient implementation of fault detection and correction in inner product computations with applications in digital signal processing algorithms; this includes FIR filters, transforms and matrix operations. The technique is based on using one extra (redundant) full channel along with another channel of much lower complexity in a modulus replication (MRRNS) processor. The MRRNS technique relies on the redundant mapping of binary input data to polynomials in indeterminates that are powers of 2. By separately computing the constant term of the output polynomial and extending the output mapping to include the redundant full channel, it is possible to correct and detect single channel errors. We have extended this technique to complex data by using a second indeterminate to represent the complex operator. By restricting the computational moduli to Fermat primes, 257 and 17, we are able to use a quadratic residue mapping in order to maintain completely independent computational channels. For a 5-channel complex MRRNS processor, a typical number for a target application in equalization filters for wireless LAN base stations, we only require approximately 30% more hardware for this fault tolerant method. The quadratic residue mapping (forward and reverse) is shown in the figure along with the computational channels.

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S6  **SIMD Architecture for MPEG Decoders**  
W. Badawy (University of Calgary)

An innovative low power SIMD architecture for MPEG decoder is designed. The architecture prototypes the mesh tools in MPEG-4 standards where affine transformation is used for motion compensation. The architecture will be used as embedded architecture for 3G cell phones and it is optimized for power consumption. Low power has been achieved by exploring the properties of the affine transformation to reduce the computational cost using mathematical transformations and finite space analysis. Moreover, the level of parallelism contributes to the reduction of the power consumption. The performance results showed that the architecture saves about 45% of the total computational operations. The behavior of the architecture is modeled using Verilog and is synthesized, simulated and analyzed using CMC-provided tools, a prototype will be fabricated using 0.35 mm TSMC technology (date for the design submission is Dec 15, 2001 and fabrication is funded by a CMC grant for $40,600). The proposed architecture can be used in video object and mesh-based motion tracking mobile applications as well as texture warping unit in graphical processors.
S7  A Novel Mesh-Based Tracking Model for Biological Cells Tracking  
K. Kaler and W. Badawy (University of Calgary)

Our work during the reporting period has been directed to the development of efficient real-time tracking of biological cells. This capability will facilitate efficient collection of real-time electro kinetic data concerning the behavior of biological cells under nonuniform electric field. We have successfully competed the following phases of the project:

- Analyzed the state-of-the arts concerning biological cells motion tracking techniques
- Developed a novel motion tracking methodology for cell tracking
- Implement the Mesh based tracking model in software to evaluate its performance
- Designed an architecture for cell identification
- Three conference papers concerning the above have been written and submitted and accepted for presentation.

The next phases of this project will concern the testing of the scheme in real-time cell processing involving the separation and/or manipulation of cells utilizing non-uniform electric fields. The developed algorithms will be implemented on silicon and integrating with the cell processing microfluidic module. This integrated capability will give rise to a novel automated cellular analysis and processing lab-on-a chip technology.

Example sequence of video frames shows the mesh growth on a moving Canola protoplast cell

S8  Median Filterin-Based Hierarchical Motion Estimation Techniques for Video Compression  
M.N.S. Swamy, M.O. Ahmad and J. Zan (Concordia University)

The conventional hierarchical motion estimation technique, although capable of reducing the heavy computational load of the full search technique, has the problem of propagating false motion vectors. In order to overcome this problem, new hierarchical motion estimation techniques making use of both the inter- and intra- resolution level motion correlations are devised. First, a neighborhood-blocks hierarchical motion estimation technique is proposed. In this technique, in order to predict a motion vector at any resolution level, the corresponding motion vector at the adjacent lower resolution level together with its neighboring motion vectors are simultaneously taken into consideration as the motion vector candidates. The proposed technique outperforms the conventional one both in terms of the prediction mean square error and the number of coding bits for the motion vectors. Next, a median filtering-based hierarchical motion estimation technique is
The proposed technique involves median filtering on a motion vector window to predict motion vectors across resolution levels. The effectiveness of this approach has been validated through its application to multi-resolution motion estimation and pyramidal motion estimation techniques. A computational analysis reveals that the additional computational load introduced by the median filtering technique is negligible. This feasibility and effectiveness have been demonstrated through extensive simulation studies.

**S9 RNS FIR Digital Filter Design and Implementation**  
M.O. Ahmad, M.N.S. Swamy and W. Wang (Concordia University)

This project explores the parallel processing methodology of using the residue number system (RNS) in the design and implementation of high-performance FIR filters. RNS DSP processors offer high-speed, low-power, and high-resolution performance for ASIC or FPGA implementations. The RNS offers carry-free and parallel operations for high-resolution and high-speed implementations. In RNS DSP processor designs, one can adjust the trade-off between speed and power.

The VLSI implementation is conducted using 0.35-micron CMOS technology. Filters are simulated and synthesized using Synopsys and Cadence tools. The FPGA implementation and test are performed using Xilinx Virtex II chip. A new look-up table scheme is applied in the design of the proposed filters. Test results show that the proposed structures deliver better performance in terms of speed and power consumption compared to binary filter structures.

**S10 Near-Optimal Multiuser Detection with Polynomial-Time Computational Complexity for Wireless Channels**  
X.M. Wang, W.-S. Lu and A. Antoniou (University of Victoria)

Demodulation in multiuser environments is crucial in multiuser wireless communications. The ML detector is shown to be optimal in terms of bit-error rate (BER) but requires exponential computation. Based on semidefinite-programming relaxation (SDPR), a new multiuser detector is developed that achieves near-optimal BER performance with reduced computational complexity. The proposed algorithm involves formulating the detection problem as an SDP problem; converting it into a dual SDP problem; and generating a binary solution from the dual SDP problem. Simulations demonstrate that the new detector can deliver near-optimal performance and is robust against near-far effects. Figure 1 illustrates the BER performance of the primal SDPR (SDPR-P) and dual SDPR (SDPR-D) detectors compared to the ML detector (MLD) for a six-user system. Figure 2 shows the CPU time required by these detectors.
S11 Beamforming Configuration for Base Station Receiver
N.Y. Wang, P. Agathoklis and A. Antoniou (University of Victoria)

The performance of different beamforming configurations for the base station receiver in CDMA systems has been studied. The results show that a better performance can be obtained when spatial diversity as well as code correlation between the interference and the signal of interest (SOI) are both considered. In the chip-based configuration, the received signal components from different antenna elements are fed into a beamformer (BF), and are then passed through a matched filter (MF). The beamforming weights are obtained by applying an optimality criterion to the received signal before despreading. In such a configuration, the interference is spatially rejected regardless of the code correlation between the interference and the SOI. Low-power interference, which is highly code-correlated to the SOI, may not be efficiently rejected. In the symbol-based configuration, a beamformer is cascaded with the MFs and the beamforming weights are determined based on the observation of the despread signal components. Spatial diversity is exploited after despreading and thus the effort applied to reject interference depends on both its power and code correlation with the SOI. As a consequence, a higher signal-to-noise-plus-interference ratio (SINR) can be obtained. Simulation results have shown that in the presence of multiple access interference, the symbol-based configuration can lead to significant improvement in the SINR relative to the chip-based configuration.

S12 Ergodic Chaos Based Spread Spectrum Watermarking Schemes
H. Leung (University of Calgary)

In this project, by exploiting the ergodic properties of deterministic chaotic signal, a novel mean-value estimation (MVE) technique based digital image watermarking scheme is proposed. In this application, a chaotic spread spectrum scheme, namely chaotic parameter modulation (CPM) is used to generate digital watermark. Instead of using spreading code, CPM is an analog spread spectrum system, which can modulate the copyright information without coding. It embeds the copyright information in the parameter of a chaotic system. The wideband signal generated from the system output is then used as watermarks to be
inserted into host images. Further, the MVE technique is applied to demodulate the CPM watermarked signal. This novel approach is shown to be superior for image watermarking in terms of noise-performance, robustness against attacks and payload by using both binary and numerical copyright information. The implementation of this scheme is simple and the computation speed is fast.

**S13 Ergodic Chaos Based Spread Spectrum Communication Schemes**  
**H. Leung (University of Calgary)**

In this project, by exploiting the ergodic properties of deterministic chaotic signal, a novel mean-value estimation (MVE) technique based spread spectrum communication schemes are proposed. Suitable non-coherent demodulator designs are developed both for digital and analog signal transmissions. Especially, a new robust communication scheme called the Ergodic Chaotic Parameter Modulation (ECPM) for digital communication is shown to have improved bit error rate (BER) performance in noisy environments and low sensitivity to multipath propagation effects.

Also the MVE technique is tested to transmit analog information signals using chaos-masking (CM) approach and proved that the performance is superior even for low signal-to-noise (SNR) ratio than that of conventional chaos synchronization based techniques. A laboratory prototype consisting MVE technique based non-coherent demodulator has been developed. This novel technique is competitive with current technology in terms of simplicity, cost-effectiveness, and design flexibility and paving ways to realize applications in chaos based WLAN, indoor radio, mobile telephony, etc.

**S14 Low Bit-Rate Audio Coder**  
**S. Krishnan and K. Umapathy (Ryerson University)**

We have developed a very low bit-rate digital audio coder by using advanced signal processing techniques. In this coder, the true non-stationary properties of the audio signal are exploited by using an adaptive time-frequency decomposition algorithm. A novel method of psychoacoustics modeling (perceptual filtering) is applied on the decomposed components. The time-frequency decomposition algorithm in combination with the psychoacoustics modeling provides very high compression ratios in the range of 7 to 30 with a wide variety of audio signals. The proposed coder provides better compression as compared to the state-of-the-coders such as MP3, but at the expense of computational complexity. Efforts are made in optimizing the algorithm for faster implementation of the coder.

**S15 Applications Architecture and CAD for a Field-Programmable System**  
**W. Chow and J. Rose (University of Toronto)**

As FPGAs push ever deeper into mainstream digital design, there is an increasing desire for high-performance circuits. We have built a new CAD tool, called EVE, which can assist a designer to perform manual packing, placement and pipelining of commercial FPGA circuits to achieve a meaningful increase in performance. This effort is inspired by Von Herzen’s work in which he made a real application work at 250MHz in a 0.7μm CMOS FPGA. It is very laborious to implement circuits using his approach; therefore we tried to augment manual design tools in order to make his methodology easier to perform.
This paper describes a first step in that direction, which focuses on placement, packing and pipelining. EVE provides an interactive environment that immediately reroutes and timing analyzes after each user circuit modification, giving an exact value for critical path delay. It can also suggest good placement positions and provide flip-flop insertion assist during pipelining. Compared to a state-of-the-art Synthesis and place and route flow, we used EVE to achieve an average of 12.7% higher operating frequency on a set of eight Xilinx Virtex-E circuits of 250 or fewer LUTs.

Picture of a screen capture of the tool, illustrating the view of the user

S16 HDL-Level Partitioning of Circuits
J.H. Rico Romo and P. Chow (University of Toronto)

The development of the Transmogrifier 3 (TM-3) at the University of Toronto has resulted in a multi-FPGA system that could be used for logic emulation. To make it useful requires the development of a partitioning tool.

The traditional approach to partitioning has been to first reduce a circuit to its fundamental components. The partitioning is then automatically performed using some heuristic procedure. This project explores the partitioning of designs at their high-level language representation, which in this case is to be able to partition a design by only using its VHDL language representation. This approach allows the designer to choose in an easy manner the partition where a component is to be placed, often to take advantage of some resource that is available to a specific FPGA such as a bank of memory or a video output. An important assumption is that large FPGAs are being used such that there are a very small number of partitions. A key result of this work is the development of a formal representation of the signal dependencies for VHDL components that makes it possible to ensure the accuracy of the tool. The partitioned design is represented as a series of VHDL files each representing one partition. Each of these files can then be processed using a regular FPGA synthesis flow.
Embedded Programmable Logic Cores provide post-fabrication flexibility to fixed-function ASIC’s. The present Micronet project is investigating the architecture of these cores, and determining how they are different than stand-alone Field-Programmable Gate Arrays. One of the primary applications of these cores is the telecom industry, where last-minute protocol changes or requirement changes are common. These applications often require wide, shallow, flexible on-chip storage. We have developed a novel architecture for these cores that contains this storage. The key concept is that we re-use the SRAM configuration bits that are normally used for storing information regarding the circuit to be implemented. For any given application, we have found that not all of these SRAM configuration bits are required to store routing information and logic information, and thus, can be used by the user to implement wide shallow storage. Compared to existing architectures, our architecture can implement this storage with a 200% increase in speed and a 15 times increase in density.

Embedded Programmable Logic Cores provide post-fabrication flexibility to fixed-function ASIC’s. These cores are different than traditional stand-alone FPGA architectures in that the programmable logic cores must be placed, along with fixed cores, onto a system-chip. The shapes and sizes of these other fixed cores, therefore, may dictate the shape and size of the programmable logic core, and may lead to programmable logic cores which are irregularly-shaped. All previous work, however, has focused on square or rectangular cores.

In order to investigate these irregularly-shaped cores, we have developed a CAD tool that can place and route circuits an L-shaped, U-shaped, and O-shaped programmable logic cores, as shown in Figures 1-3. There were two main challenges in creating this tool: (1) we developed a method for specifying these irregularly-shaped cores, and (2) we modified and optimized standard placement and routing algorithms to create smaller and faster circuit implementations within the programmable logic core. This is the first such publicly-available CAD tool, and we have made it available to the Canadian and international research community.
With the development of ASIC/SOC designs, simulation cannot cover all the corner cases in a complicated design flow. Model checking is a fully automatic approach to verify a finite state machine against its temporal specifications. However, its application is limited by the size of the system to be verified. Compositional verification and model reduction are two possible methods to tackle this problem. We have developed a formal verification framework based on assume-guarantee compositional reasoning and a new model reduction approach. In this framework, temporal specifications are synthesized into Verilog modules, and local properties are composed into global properties. In case a module under verification is beyond the capability of model checking, the proposed model reduction algorithm can be used. We implemented the framework on top of the VIS tool from UC Berkeley and applied it on an ATM switch fabric from Nortel Networks. Throughout this case study, we have been able to discover some errors in the design.
The Syslib-Picasso Methodology for the Co-Design Capture Phase
G. Bois (École Polytechnique de Montréal) and E.M. Aboulhamid (Université de Montréal)

This project works on the development of Syslib, a high-level C++-based library for designing embedded systems. Syslib splits the specification capture phase into three distinct levels: A designer captures a specification respecting pre-defined constructs representing the system semantics and refines his descriptions to reach the implementation languages. The functional level allows the definition of the main algorithm of an application at an untimed high level of abstraction. The behavioral level introduces the notion of time and the scheduling of the algorithm’s modules. Finally, in the third level, Syslib helps a designer to map to an architecture by providing a complete API to link software modules with a real-time operating system and to support hardware blocks with module intercommunications. Validation of specifications at a high level decreases simulation time. Once the capture finished, the system is ready to be co-verified with commercial tools, like MTI ModelSim and Mentor Graphics’ Seamless CVE. Syslib takes place in a complete co-design methodology called Picasso. Results to be expected from the methodology are a shorter development time period by efficient refinement steps with less translation errors.

Syslib does not claim to compete with existing languages like SystemC. First, Syslib is intended to be a complementary language to Cynlib from Forte Design Systems, in order to work at the system level. Also, the integration of Syslib in a complete function-architecture co-design methodology strengthens its efficiency and interest. One of the goals of this work is to provide a good source of inspiration for people working on C/C++ standardization efforts at system level (e.g. Accelerra).

The complete Syslib-Picasso methodology
S21 Modeling and Optimization or Critical SoC Components
Z. Zilic, I. Brynjolfson, B. Polianskikh, H. Chan, S. McCracken, A. Chattophadyay, M.-W. Chieng, M. Boule and K. Radecka (McGill University)

We have established a viable platform for low-power design using variable-rate clock management and have tested it in a series of integrated circuits. A complete Managed Clock System on Chip (McSoC) implementation was built that employs these low power techniques. The McSoC implementation includes a novel range-shifting PLL (RSPLL) that is optimized for dynamic clock reconfiguration. The RSPLL design is shown to scale well to low voltage and high bandwidth. Next, we have created an efficient modeling algorithm for the substrate coupling between digital and analog subsystems that employs the optimal Voronoi construction of the equivalent circuit. Further, fault tolerant memories and programmable logic devices were designed employing the novel codes and the architecture of the redundant parts that increases the reliability and the manufacturing yield, while keeping the speed and energy consumption within the bounds of the non-redundant circuit, hence making it easier to incorporate at a system level.

S22 Combining Formal and Simulation Verification
Z. Zilic and K. Radecka (McGill University)

We concentrated on providing the infrastructure for combining the formal and simulation-based approaches, which has promise of surpassing the limitations of both approaches used in isolation.

Significant results have been obtained in verification of datapaths, where we demonstrated usefulness of the Arithmetic Transform (AT) as a concise canonical circuit representation. In verification by testing, we have proven a fundamental theorem on the use of Arithmetic Transform in the Universal Test Set (UTS) for detection of the designer and tool errors. Additionally, the first known exact algorithm for detecting wide classes of redundant design errors has been presented, together with the series of useful approximations. We have also recently presented a new method for formal verification of sequential arithmetic systems and their compositions. Together, these two advances create a viable combination of formal verifications with simulation-based approaches that is based on the same AT underlying representation.

S23 SystemC Evaluation and Use in Modeling System-On-Chip Designs
E.M. Aboulhamid (Université de Montréal) and G. Bois (École Polytechnique de Montréal)

SystemC is a hardware description language and open source environment based on C++. We introduced a hardware modeling methodology based on the object oriented and multi-paradigms capabilities of SystemC. We based this methodology on the concepts of commonality and variation developed in the Software Engineering area. We have also shown the similarity of problems and solutions between the design patterns methodology and IP reuse in hardware. All these Software Engineering concepts facilitate reuse in the System-On-Chip domain. Simulation performance is also an important issue, given the complexity of the modelled systems. In collaboration with STMicroelectronics, we used SystemC to model a pipelined multiprocessor at a cycle accurate level. We evaluated the impact of the complexity of the models as well as different modeling approaches on the simulation performance. Our models have been also sent to an Italian and a German
University to be used in their advanced Computer Architecture courses and research projects. Finally, we developed a methodology for automatic documentation of SystemC environment. This is used and available worldwide through our website. The Open SystemC Initiative, the organization responsible of SystemC development and distribution, is aware of our efforts and refers to our website.